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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/724,009	LINDOLF ET AL.
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-20 and 27-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-20 and 27-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration, through persuasive arguments with respective to the 102/103 rejection over the Takagi reference, of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Election/ Restriction

2. Applicant's election without traverse of Group I, claims 14-20, cancellation of claims 1-13 and 21-26, and addition of claims 27-45, in the reply filed on 07/18/2005, is acknowledged. New claims 27-45 are sufficiently non-restrictable from elected claims; accordingly, claims 14-20 and 27-45 are under examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "substrate" in "wherein the first conductive region and the nonconductive region are formed in a substrate for forming the antifuse structure" of **claims 27, 32, 40, and 43** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The new claims and the withdrawal of the previous rejection have necessitated new grounds of rejection as follow.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 14-15, 17-20, 28-30, 34-39, 41, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Hawley et al. U.S. Patent 5,920,109 (the '109 reference).

The '109 reference discloses in Figure 1 and respective portions of the specification an antifuse and a method for producing and blowing thereof as claimed.

Referring to **claims 14, 17, 28-29, 35-36, 38-39, and 41**, the '109 discloses an antifuse and a method for producing and blowing thereof, comprising:

a first conductive region (18, column 3, lines 15-22), the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge **or a corner** ("edge" is interpreted broadly);

a nonconductive region (16, column 3, lines 8-15) adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface;

a dielectric layer (22, column 3, lines 40-45) disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer **proximate the corner** (column 3, lines 28-30); and a

second conductive region (34, column 4, lines 12-15) on the dielectric layer.

Referring to **claims 15, 30, and 37**, the reference further discloses that the first conductive region (18) defines a corner (corner is interpreted broadly) and wherein the dielectric layer (22) is disposed over the corner.

Referring to **claims 18-20, 34, and 45**, the reference further discloses that the nonconductive region comprises SiO_2 ("silicon dioxide", column 3, lines 8-12), meeting the limitation of the claimed Markush group of at least one of SiO_2 and SiN, and wherein the dielectric layer comprises SiN ("silicon nitride", column 3, lines 42-45).

6. **Claims 14, 17, 28-29, 31, 35-36, 38-39, and 41-42** are rejected under 35 U.S.C. 102(b) as being anticipated by Go et al. U.S. Patent 5,592,016 (the '016 reference).

The '016 reference discloses in Figures 14-15 and respective portions of the specification an antifuse and a method for producing and blowing thereof as claimed.

Referring to **claims 14, 17, 28-29, 35-36, 38-39, and 41**, the '016 discloses an antifuse and a method for producing and blowing thereof, comprising:

a first conductive region (218, column 11, lines 35-38), the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge **or a corner**;

a nonconductive region (214) adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface;

a dielectric layer (220) disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer **proximate the corner** (similar to the '109 reference cited above, the property "whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer" is inherent in the device, although Go does not explicitly disclose); and a

second conductive region (224) on the dielectric layer.

Referring to **claims 31 and 42**, the reference further discloses that the first lateral boundary surface is substantially orthogonal to a lower surface of the dielectric layer (220) interfacing with the edge.

7. **Claims 14, 16-17, 28-29, 35, and 41** are rejected under 35 U.S.C. 102(b) as being anticipated by Gordon et al. U.S. Patent 5,880,512 (the '512 reference).

The '512 reference discloses in Figure 5 and respective portions of the specification an antifuse and a method for producing and blowing thereof as claimed.

Referring to **claims 14, 17, 28-29, 35, and 41**, the '512 discloses an antifuse and a method for producing and blowing thereof, comprising:

a first conductive region (545, column 8, lines 20-22), the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge **or a corner**;

a nonconductive region (540, column 8, lines 23-25) adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface;

a dielectric layer (25) disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel (210) in the dielectric layer **proximate the corner** ("proximate" is interpreted broadly, and although the reference does not explicitly disclose "an area of relatively increased field strength is produced during application of a programming voltage", an area of relatively increased field strength is produced during application of a programming voltage because the area of relatively increased field strength produces the breakdown channel 210, as is known by a person of ordinary skill in the art); and a

second conductive region (26 or 27) on the dielectric layer.

Referring to **claim 16**, the reference further discloses that the first conductive region (545) and the nonconductive region (540) form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer (25).

Claim Rejections - 35 USC § 102 and/or § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. **Claims 14-20, 28-30, 34-39, 41, and 45** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hawley et al. U.S. Patent 5,576,576 (the '576 reference).

The '576 reference discloses in Fig. 1 and respective portions of the specification an antifuse and a method for producing and blowing thereof as claimed or substantially as claimed.

Referring to **claims 14, 17, 28-29, 35-36, 38-39, and 41**, the '576 discloses an antifuse and a method for producing and blowing thereof, comprising:

a first conductive region (20, column 4, lines 53-56), the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge **or a corner**;

a nonconductive region (16 or 22, column 4, lines 37-40 or lines 34-59) adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface;

a dielectric layer (24, paragraph bridging columns 4 and 5) disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface; and a

second conductive region (26, column 5, lines 10-15) on the dielectric layer.

The reference, however, does not disclose the property whereby an area of relatively increased field strength is produced in the dielectric layer and along the edge during application of a programming voltage to form a breakdown channel in the dielectric layer **proximate the corner".** Nevertheless, comparing the present invention structure (Figs. 1-4) and the structure of the '576 reference (Fig. 1), the structure of the '576 reference comprises all the elements of the structure of the present invention therefore the structure of the '576 reference should also comprise all of the properties of the structure of the present invention, including the property whereby an area of relatively increased field strength is produced in the dielectric layer and along the edge during application of a programming voltage to form a breakdown channel in the dielectric layer proximate the corner.

Referring to **claims 15, 30, and 37**, the reference further discloses that the first conductive region (18) defines a corner and wherein the dielectric layer (22) is disposed over the corner.

Referring to **claim 16**, the reference further discloses that the first conductive region (20) and the nonconductive region (16 or 22) form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer (24).

Referring to **claims 18-20, 34, and 45**, the reference further discloses that the nonconductive region (16) comprises SiO_2 ("silicon dioxide", column 4, lines 37-41), meeting

the limitation of the claimed Markush group of at least one of SiO_2 and SiN, and wherein the dielectric layer (24) comprises SiN ("silicon nitride", paragraph bridging columns 4 and 5).

9. **Claims 14-20 and 27-45** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Peng U.S. Patent 6,700,151 (the '151 reference).

The '151 reference appears to disclose in Fig. 4 and respective portions of the specification an antifuse and a method for producing and blowing thereof as claimed.

Referring to **claims 14, 17, 28-29, 33, 35-36, 38-39, 41, and 44**, the '151 discloses an antifuse (capacitor 425) and a method for producing and blowing thereof, comprising:

a first **doped-semiconductor** (claims 33 and 44) conductive region (406, column 6, last paragraph), the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge **or a corner** ("edge" is interpreted broadly);

a nonconductive region (302, column 6, lines 5-8) adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface;

a dielectric layer (312, column 6, lines 40-45) disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion of the second upper surface; and a

second conductive region (301) on the dielectric layer.

The reference, however, does not disclose the property whereby an area of relatively increased field strength is produced in the dielectric layer and along the edge during application of a programming voltage (which cause an electrical current to flow form conductive electrode region 301, through dielectric layer 312, to doped semiconductor conductor region 406, to source/drain 306) to form a breakdown channel in the dielectric layer proximate the corner". Nevertheless, comparing the present invention structure (Figs. 1-4) and the structure of the '151 reference (Fig. 4), the structure of the '151 reference comprises all the elements of the structure of the present invention therefore the structure of the '151 reference should also comprise all of the properties of the structure of the present invention, including the property whereby an area of relatively increased field strength is produced in the dielectric layer and along the edge during application of a programming voltage to form a breakdown channel ("breakdown channel" is interpreted broadly, as in the instant case, a "breakdown channel " means a conduction path in the normally nonconductive dielectric layer 4 of the present invention and a conduction path in the normally nonconductive dielectric layer 312 of the '151 reference; or as disclosed as "soft or hard breakdown", the '151 reference, columns 1 through 4, particularly column 4, lines 10-20) in the dielectric layer (312) proximate the corner.

Referring to **claims 15, 30, and 37**, the reference further discloses that the first conductive region (406) defines a corner and wherein the dielectric layer (312) is disposed over the corner.

Referring to **claim 16**, the reference further discloses that the first conductive region (406) and the nonconductive region (302) form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer (312).

Referring to **claims 27, 32, 40, and 43**, the reference further discloses that the first conductive region (406) and the nonconductive region (302) are formed in a substrate (313) for forming the antifuse.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 14-20, 28-31, 34-39, 41-42, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al. U.S. Patent 5,625,219 (cited in a previous office action).

Takagi discloses in Figures 1-6 and respective portions of the specification an antifuse and a method for producing and blowing thereof substantially as claimed.

Specifically, Takagi discloses a single region 7 that is functionally equivalent to the nonconductive region 2 and the dielectric layer 4 of the present invention. More specifically and with reference to Figs. 5C and 6, with added reference characters as depicted on the following page for ease of explanation, Takagi discloses an antifuse, comprising:

a first conductive region (62), the first conductive region defining a first upper surface (62US) and a first lateral boundary surface (SS) which meet at an angle (62C) to form an edge;

a nonconductive region (7B) adjoining the first conductive region (62), the nonconductive region defining a second upper surface and a second lateral boundary surface

(SS); wherein the first and second lateral boundary surfaces are in facing relationship and form an interface (generally indicated as SS);

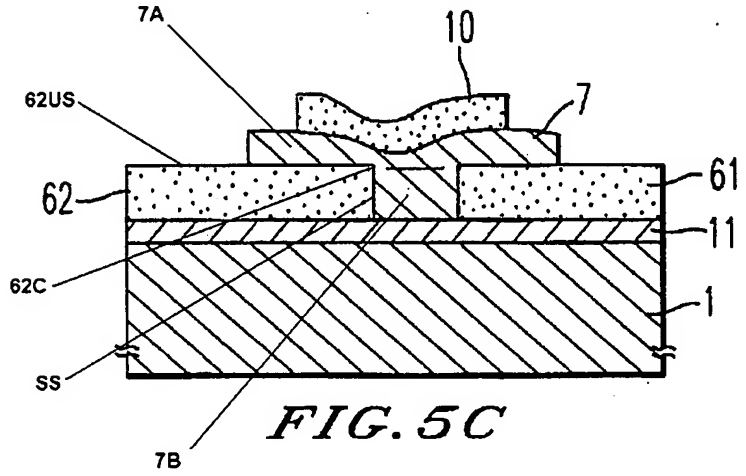

FIG. 5C

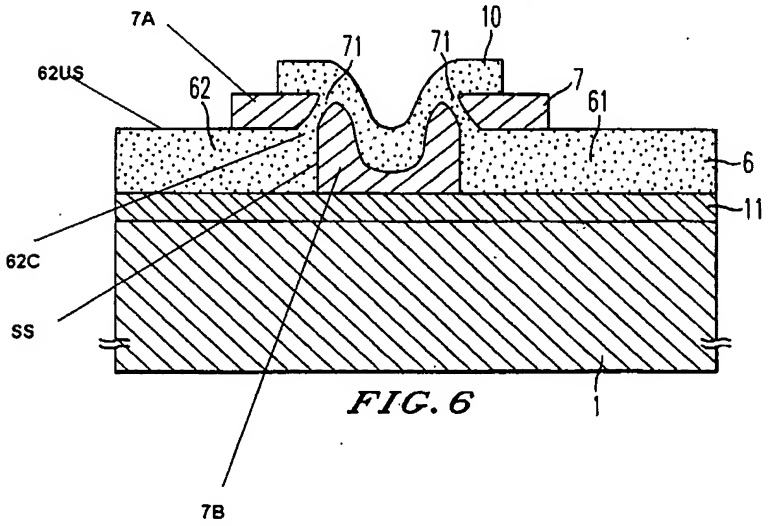

FIG. 6

a dielectric layer (7A) disposed over at least a portion of the first upper surface (62US) of the first conductive region and at least a portion of the edge (62C), whereby an area of relatively increased field strength is produced during application of a programming voltage to form a

breakdown channel (71) in the dielectric layer; and a second conductive region (10) on the dielectric layer.

As noted, Takagi discloses a single region 7 that is functionally equivalent to the nonconductive region 2 and the dielectric layer 4 of the present invention. Although the claimed invention is not identically disclosed or described by Takagi, the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. The subject matter as a whole, providing a dielectric region (7) including a dielectric portion (7A) and a nonconductive region (7B), as disclosed by Takagi, or providing a dielectric region including a dielectric layer (4) and a nonconductive region (2), as claimed, so that an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric portion (7A) or dielectric layer (4) would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains, simply because neither variation, namely providing a dielectric region (7) including a dielectric portion (7A) and a nonconductive region (7B), as disclosed by Takagi, or providing a dielectric region including a dielectric layer (4) and a nonconductive region (2), as claimed, produces a product that is a newer or a useful improvement thereof over the other.

Referring to **claims 15, 30, and 37**, Takagi further discloses that the conductive region (62) defines a comer (62C) and wherein forming the dielectric layer (7A) comprises forming the dielectric layer over the comer. Referring to the limitation "area of relatively increased field strength" of claim 37, the area of relatively increased field strength results in the breakdown of the dielectric layer 7A at the corner and the eventual forming of the path 71).

Referring to **claim 16**, Takagi further discloses that the first conductive region (62) and the nonconductive region (7B) form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer (7A, best seen in Fig. 5C).

Referring to **claims 18-20, 34, and 45**, Takagi further discloses that the nonconductive region (7B) comprises SiN and the dielectric layer (7A) comprises SiN (column 6, lines 61-63).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
September 07, 2005